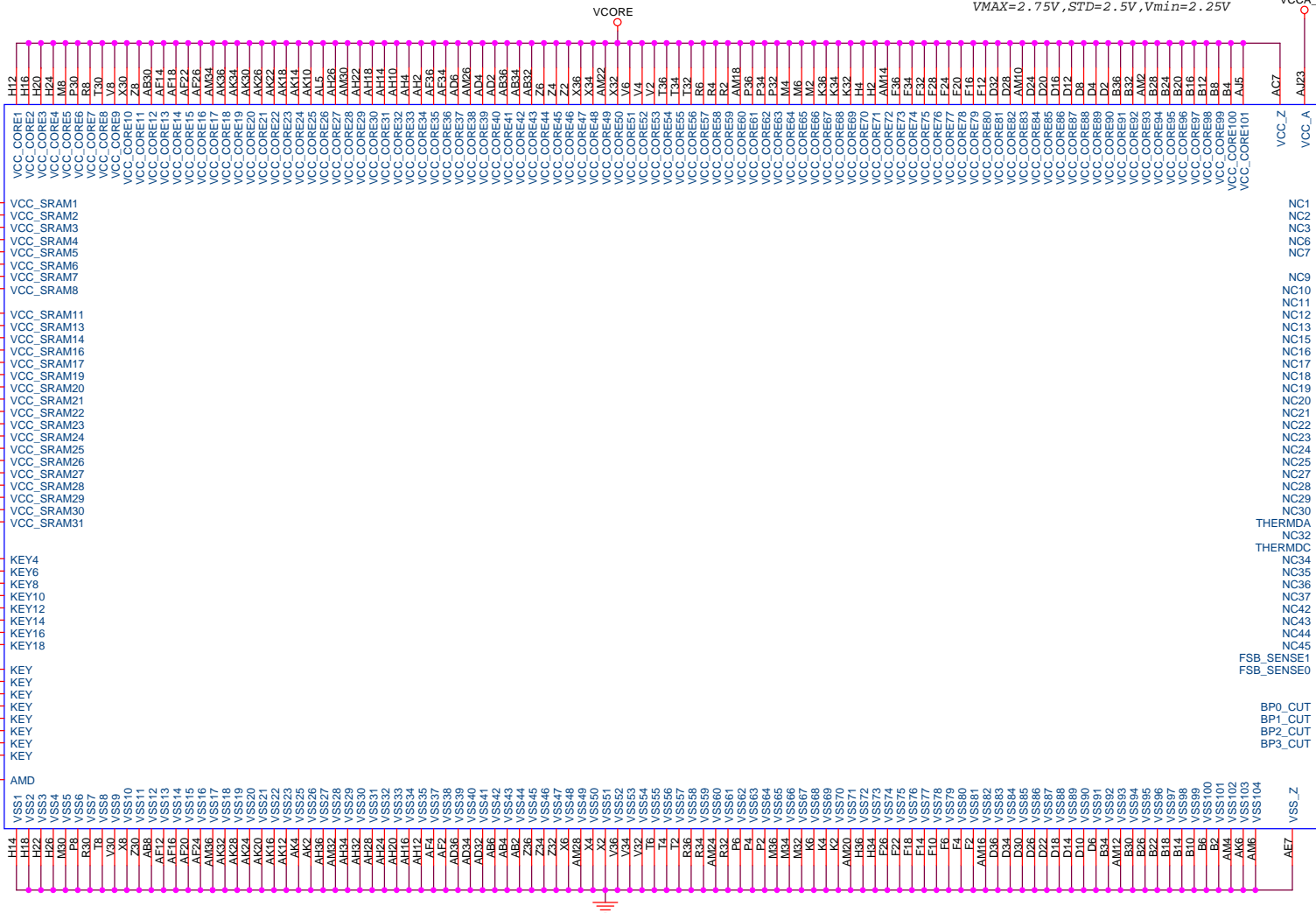
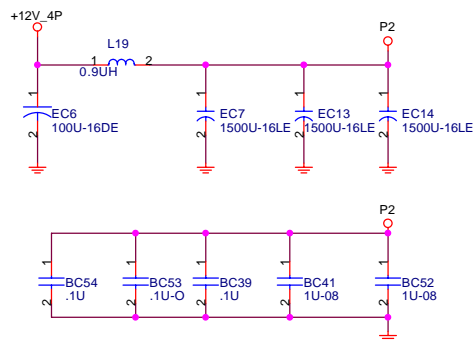
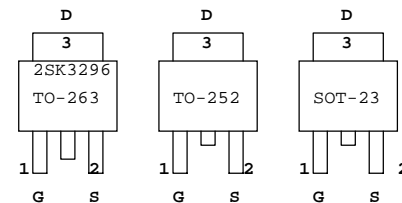
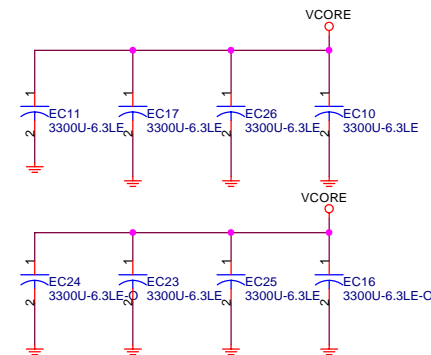
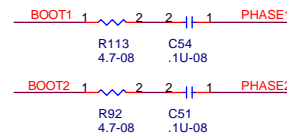
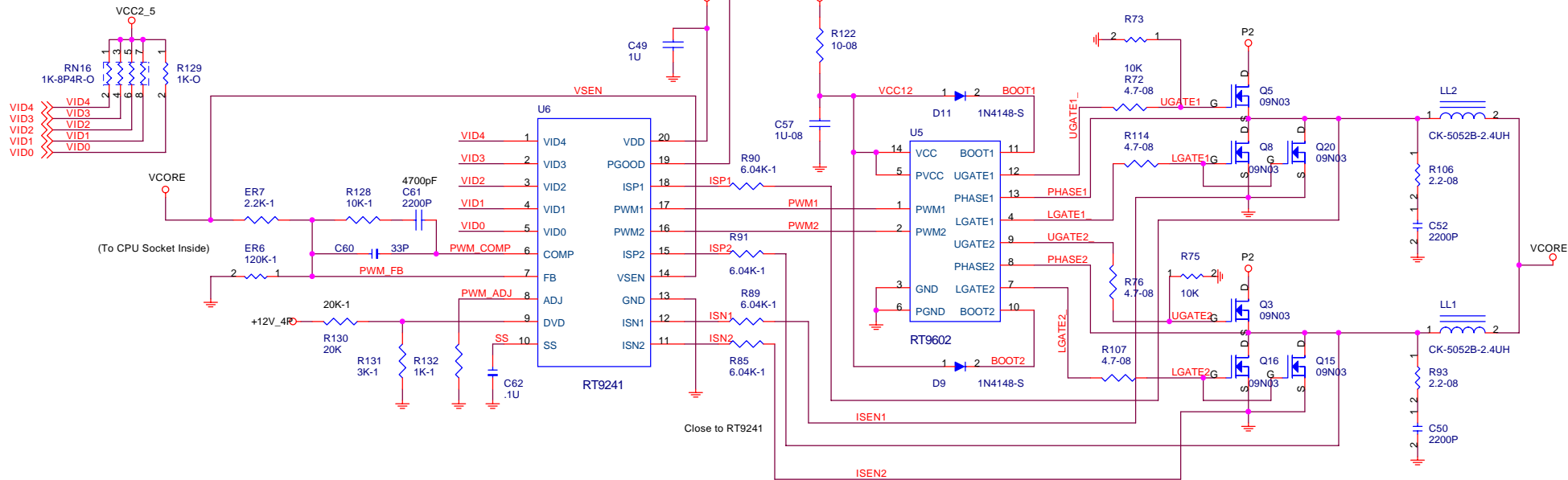


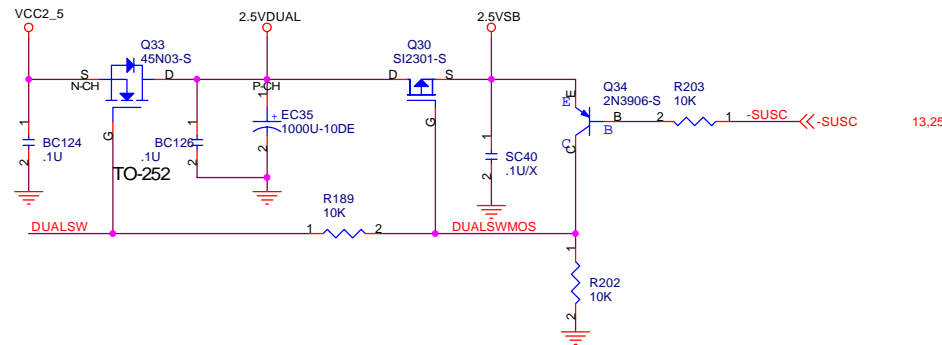
AD30 VCC\_SRAM1  
 AD8 VCC\_SRAM2  
 AF10 VCC\_SRAM3  
 AE28 VCC\_SRAM4  
 AF30 VCC\_SRAM5  
 AF32 VCC\_SRAM6  
 AF6 VCC\_SRAM7  
 AF8 VCC\_SRAM8  
  
 AH8 VCC\_SRAM11  
 AJ9 VCC\_SRAM13  
 AK8 VCC\_SRAM14  
 AL9 VCC\_SRAM16  
 AM8 VCC\_SRAM17  
 F30 VCC\_SRAM19  
 F8 VCC\_SRAM20  
 H10 VCC\_SRAM21  
 H28 VCC\_SRAM22  
 H30 VCC\_SRAM23  
 H32 VCC\_SRAM24  
 H6 VCC\_SRAM25  
 H8 VCC\_SRAM26  
 K30 VCC\_SRAM27  
 K8 VCC\_SRAM28  
 AJ7 VCC\_SRAM29  
 AL7 VCC\_SRAM30  
 AN7 VCC\_SRAM31  
  
 G25 KEY4  
 G17 KEY6  
 G9 KEY8  
 N7 KEY10  
 Y7 KEY12  
 AG7 KEY14  
 AG15 KEY16  
 AG29 KEY18  
  
 G7 KEY  
 Q7 KEY  
 AA7 KEY  
 AG9 KEY  
 AG17 KEY  
 AG27 KEY  
 G15 KEY  
 G23 KEY  
  
 AH6 AMD



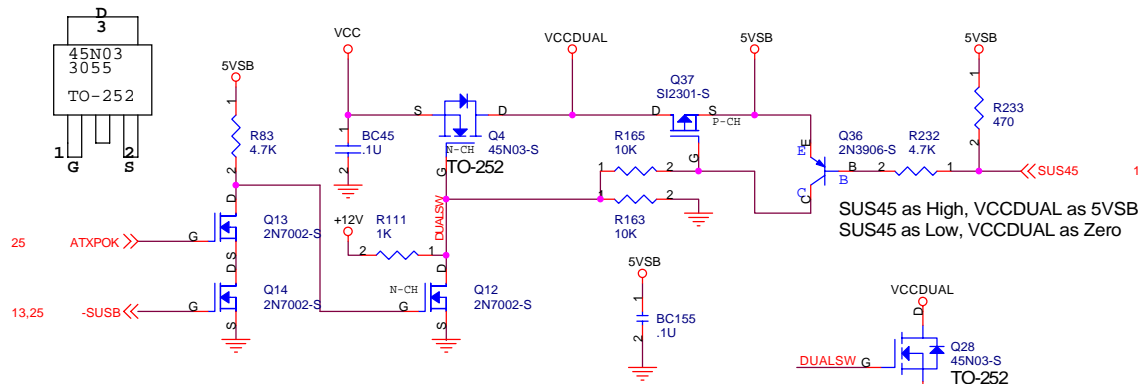
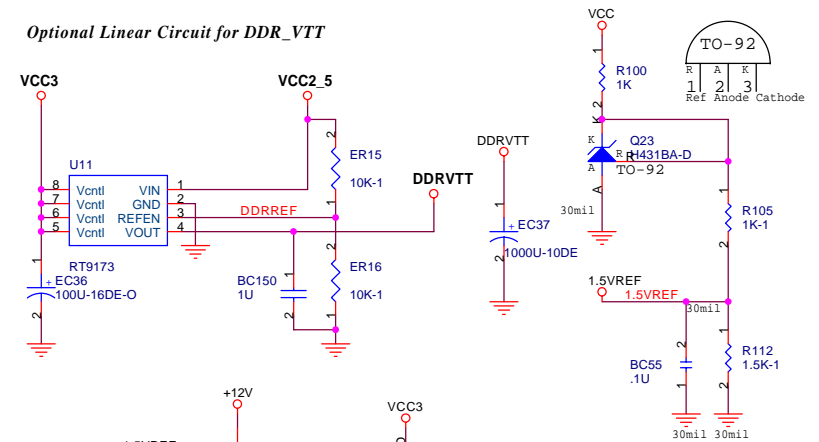


1  
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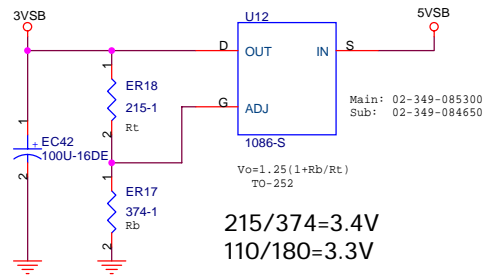




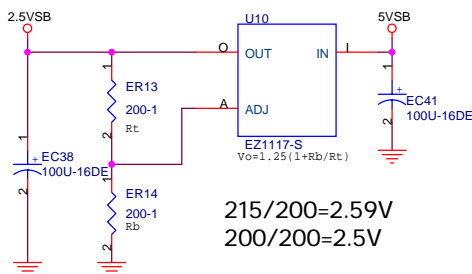
Optional Linear Circuit for DDR\_VTT



### 3.3V Stand-By

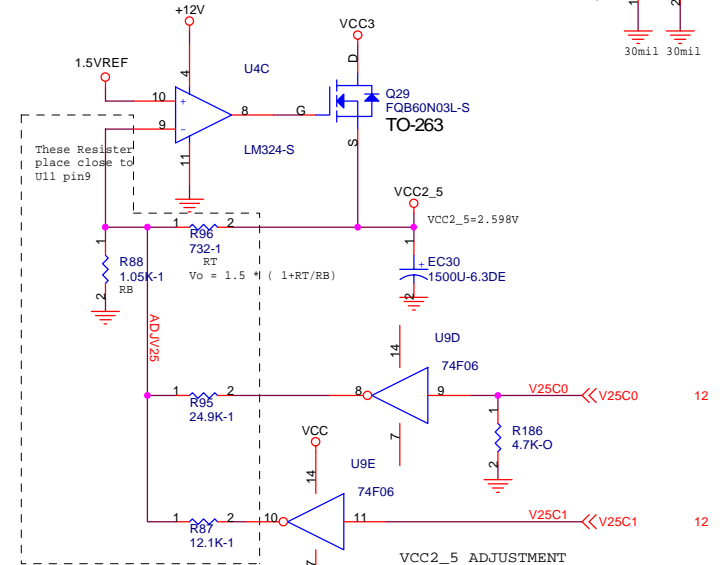


### 2.5V Stand-By

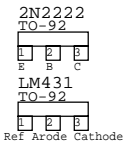
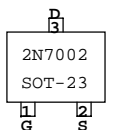
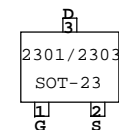


Note:

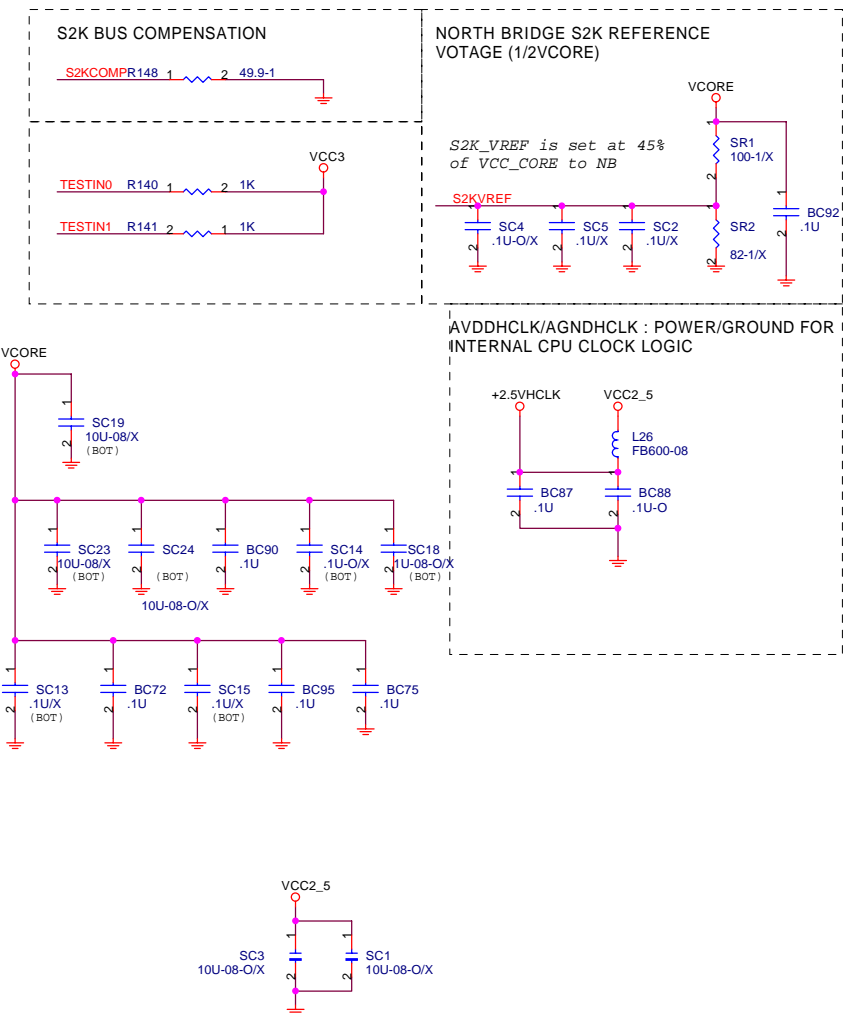
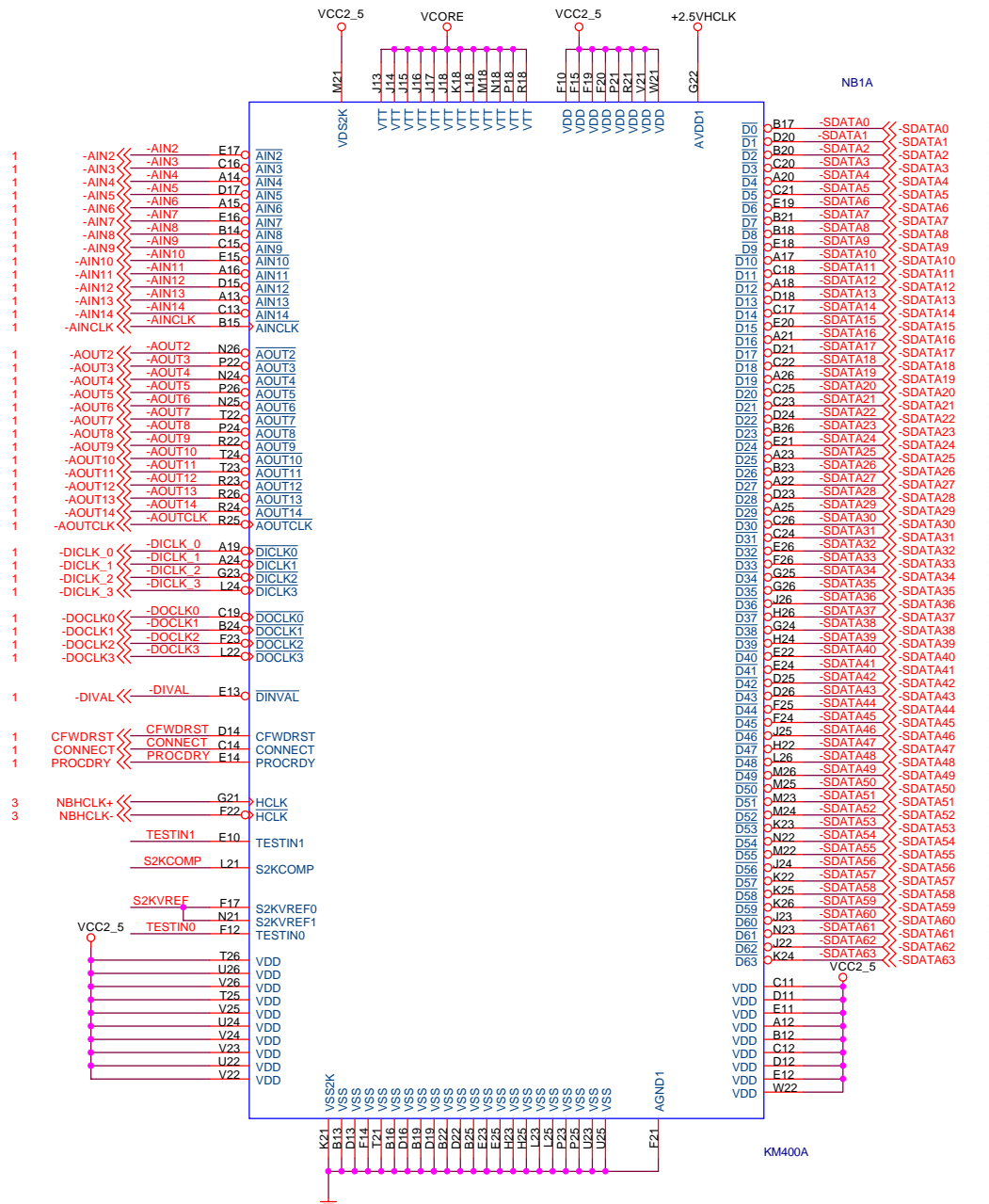
MODE	RSMRST-	SUST-	-SUSA	-SUSB	-SUSC
OFF	0	0	0	0	0
S0(ON)	1	0	1	1	1
S1	1	0	0	1	1
S3	1	0	0	0	1
S4/S5	1	0	0	0	0



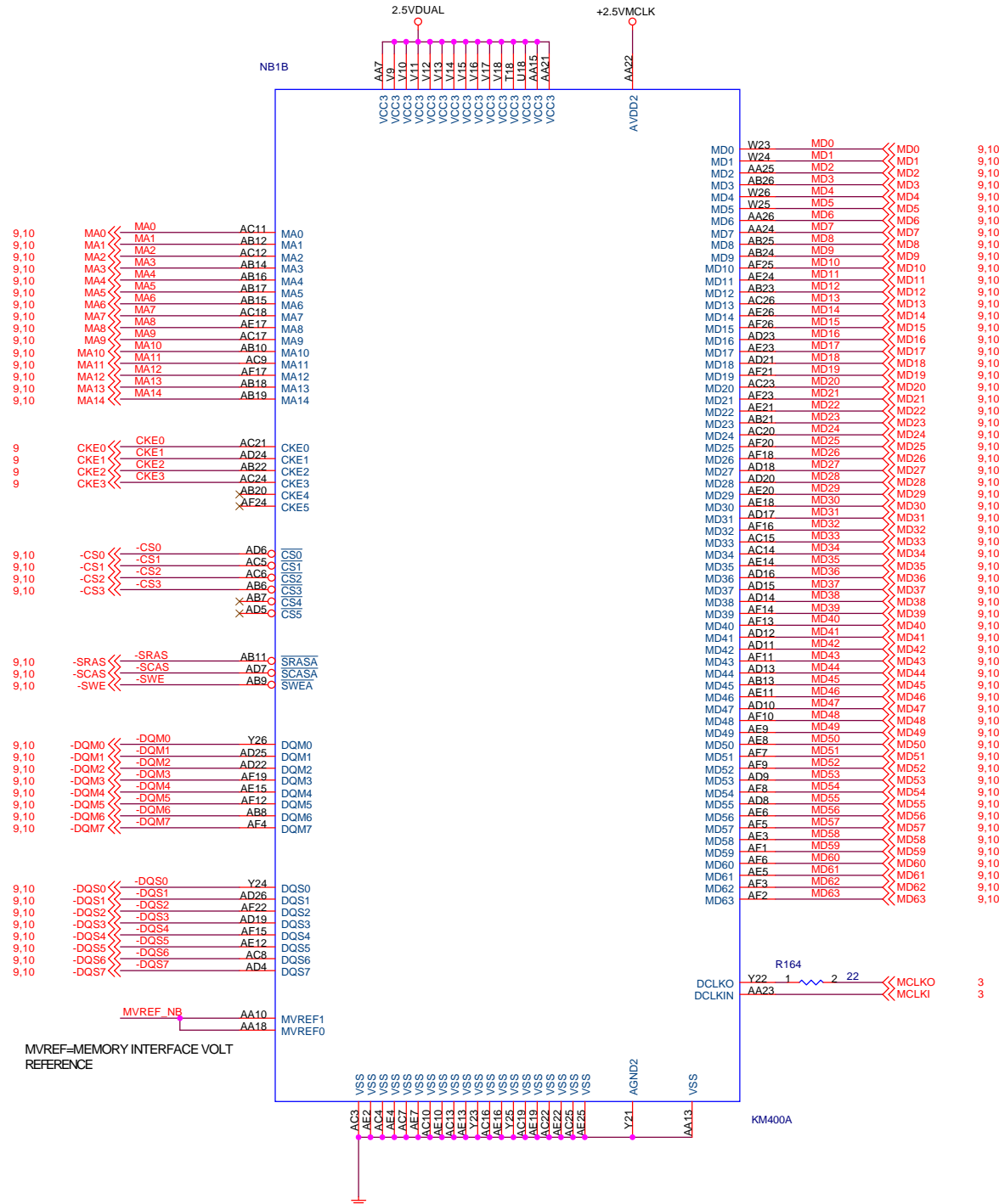
V25C1	V25C0	VCC2_5
0	0	2.54V
0	1	2.58V
1	0	2.63V
1	1	2.67V



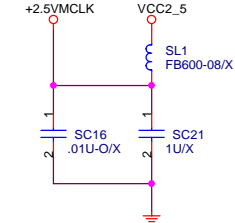
NORTH BRIDGE 1 of 3 ( HOST BUS)



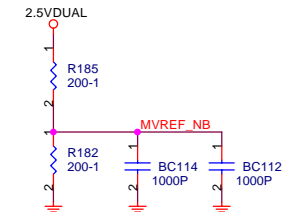
# NORTH BRIDGE 2 of 3 ( MEMORY)



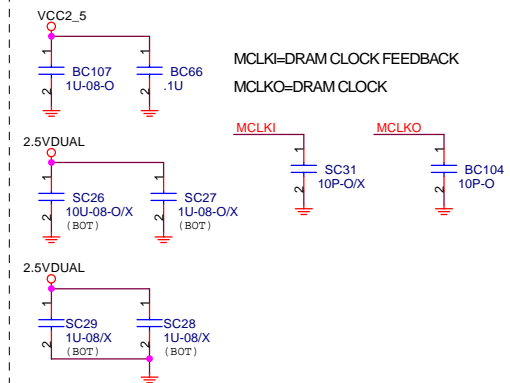
## AVMCLK/AGNDMCLK : POWER/GROUND FOR DRAM CLCOK DESKEW CIRCUIT



## MVREF\_NB : SSTL\_2 RECEIVER VREF FOR DDR



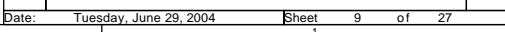
## 25VDUAL : +2.5V LEVEL DRAM POWER



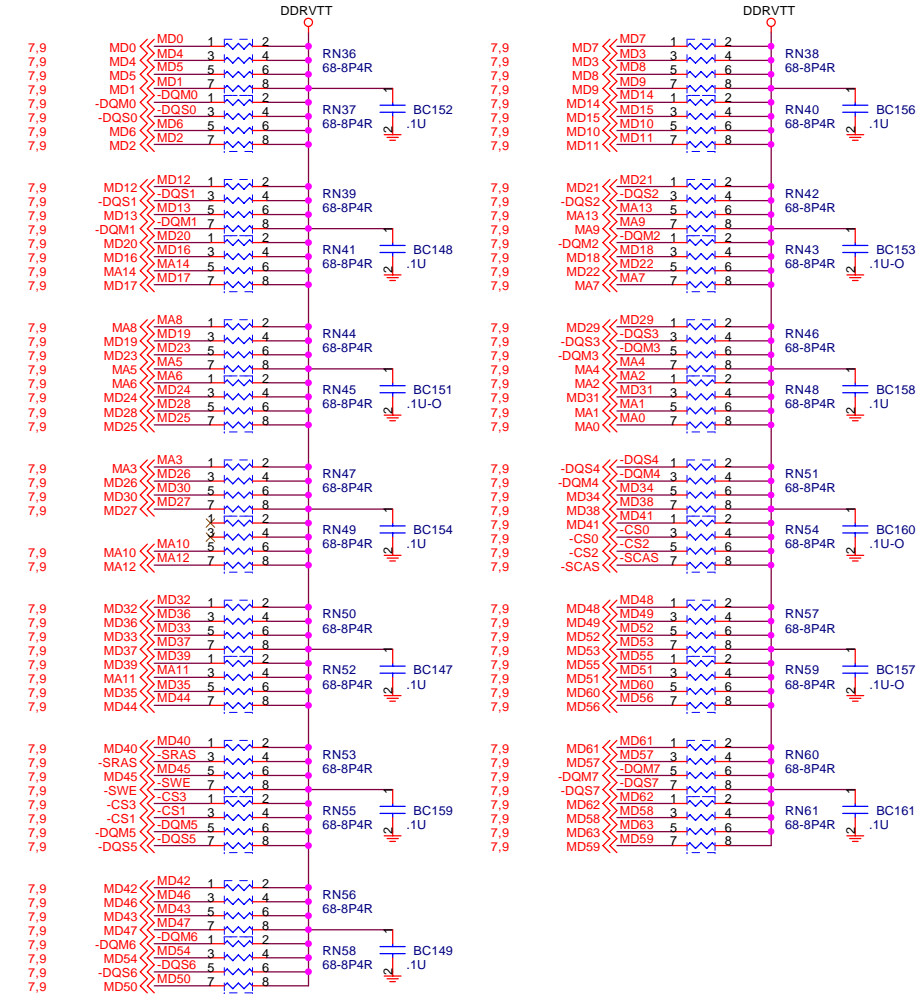
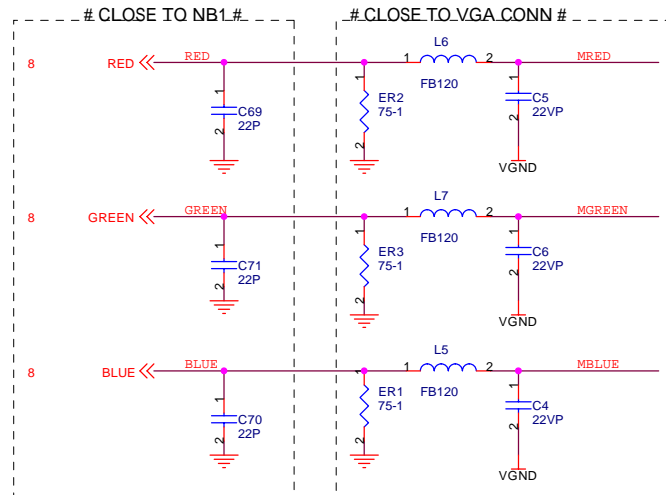
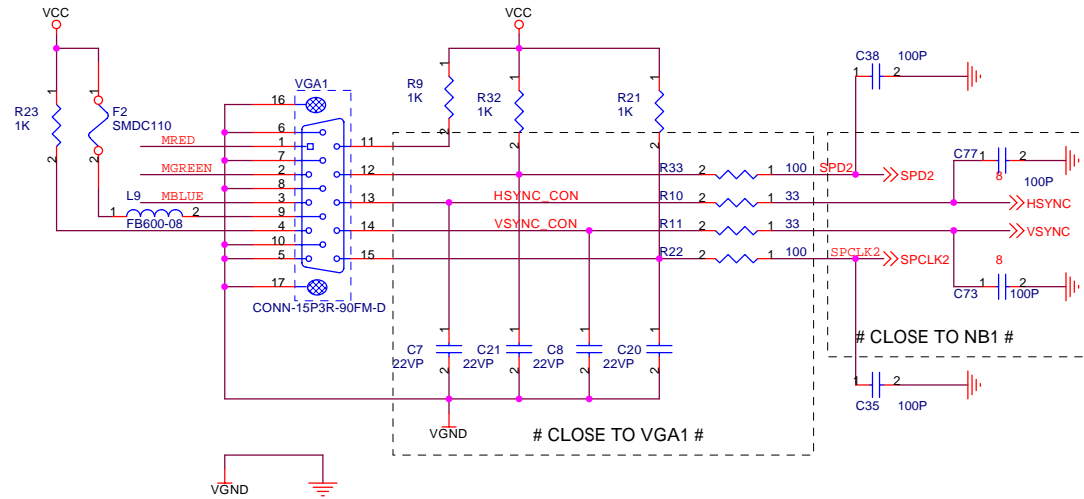




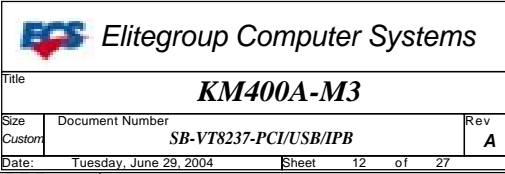


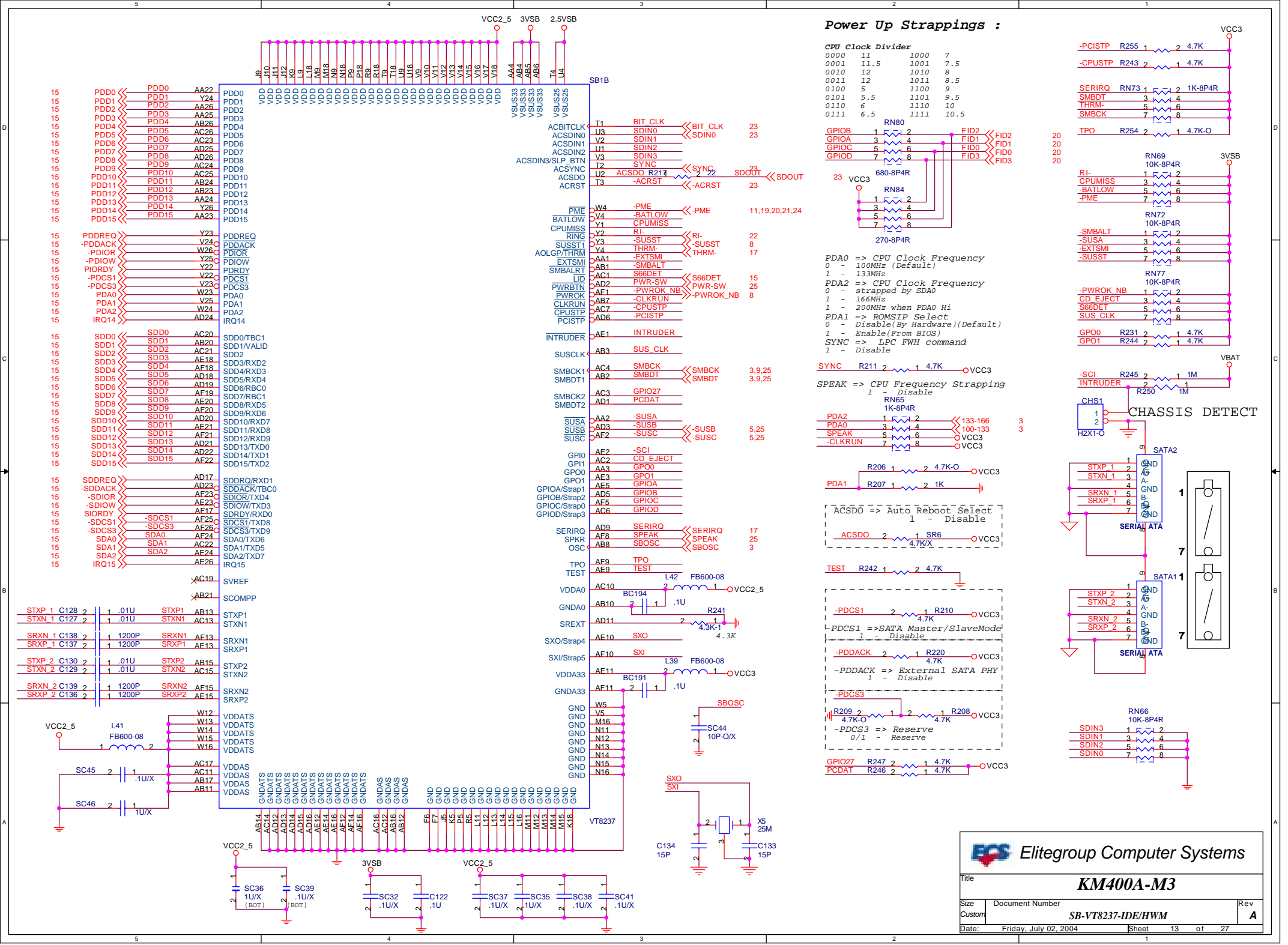


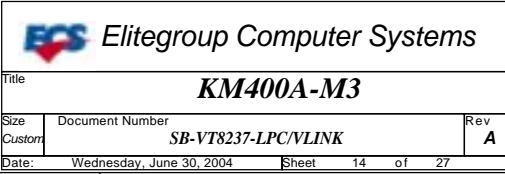
# VGA CONN.







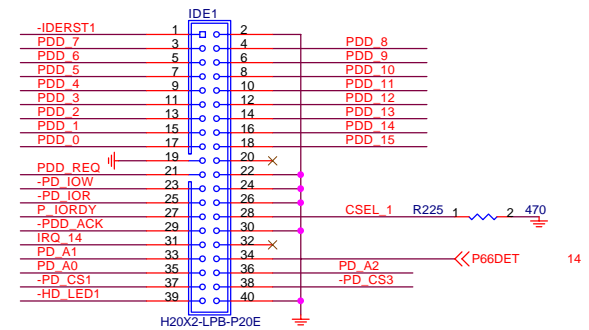
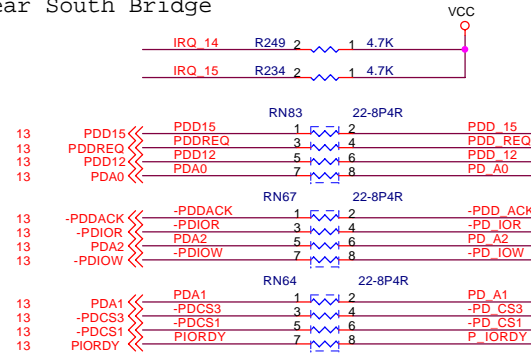
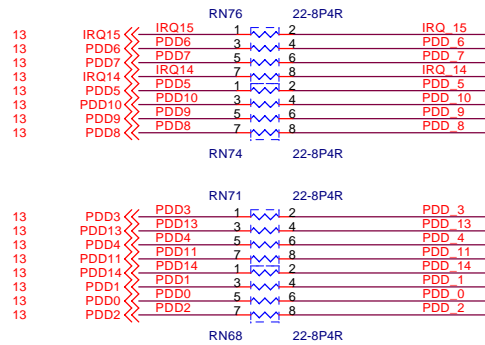






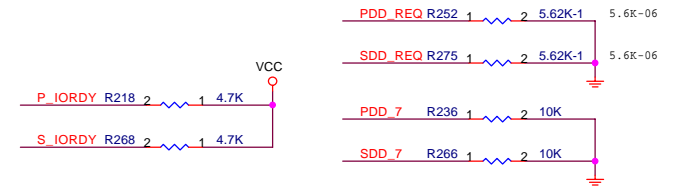
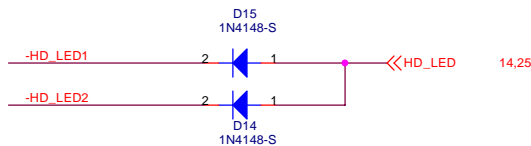
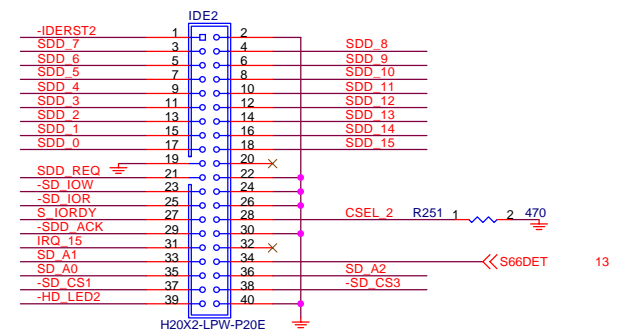
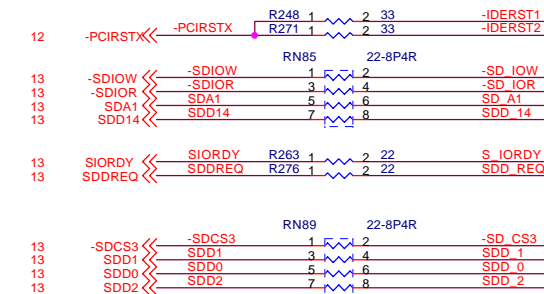
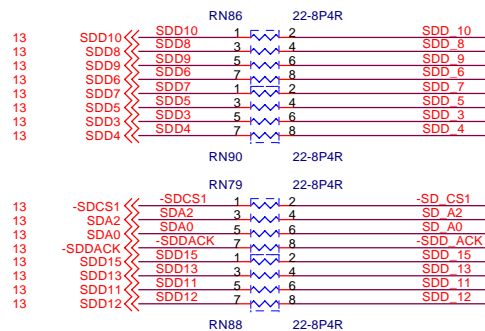
# PRIMARY

These resistor should placed near South Bridge



# SECONDARY

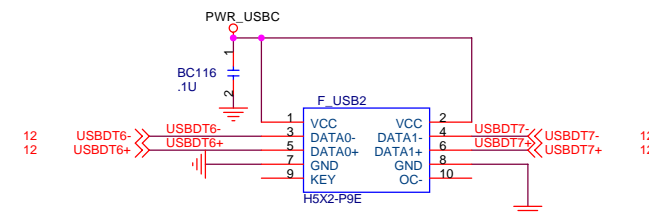
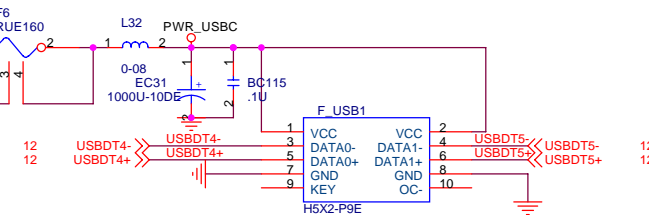
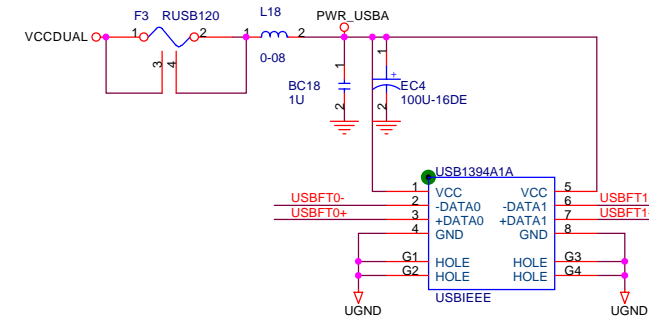
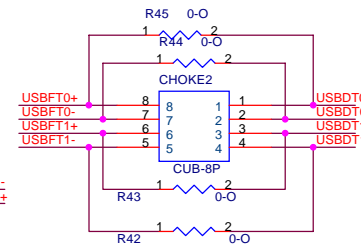
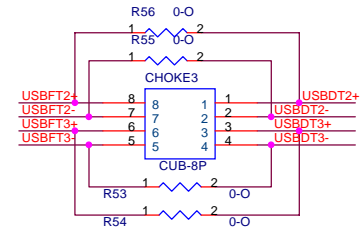
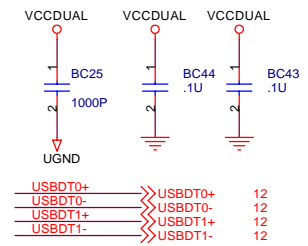
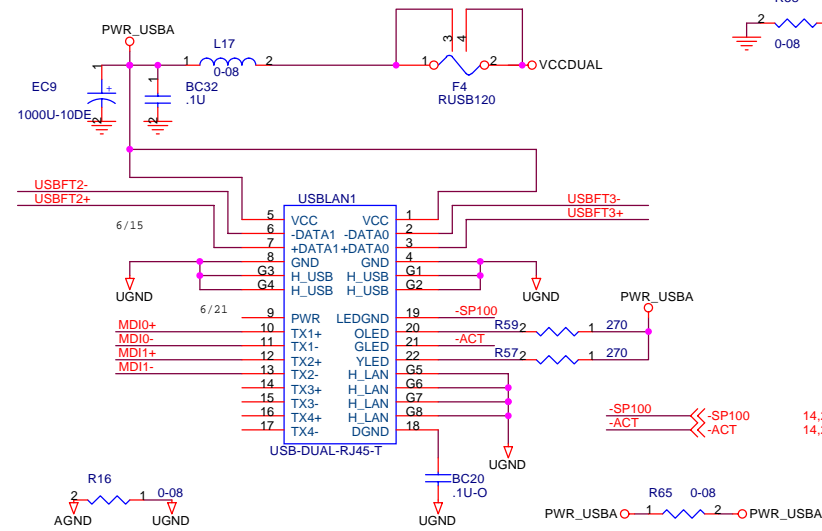
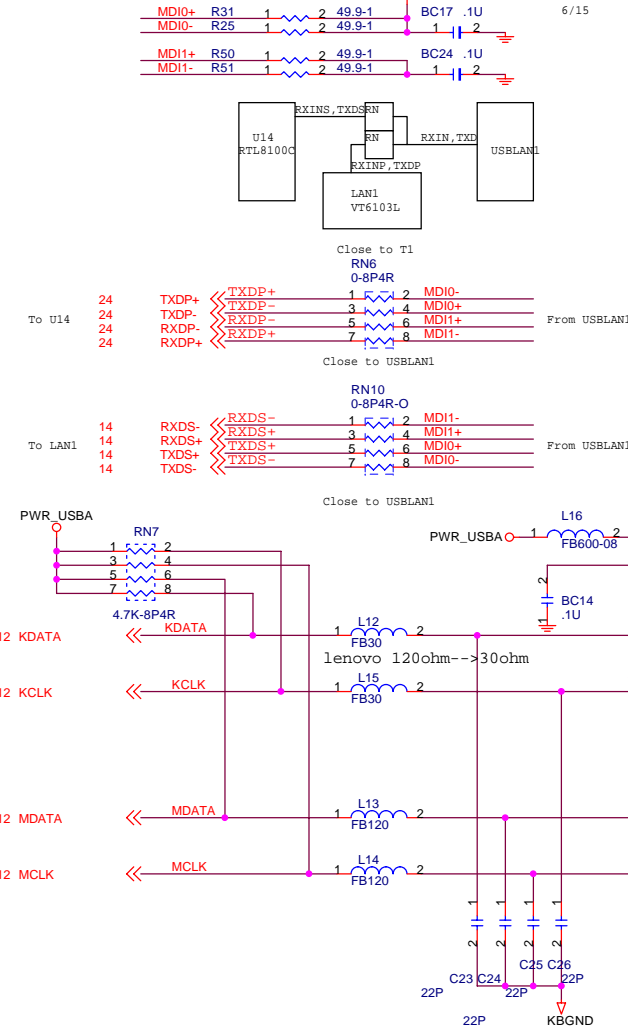
These resistor should placed near South Bridge



Elitegroup Computer Systems



## USB PORT INTERFACE

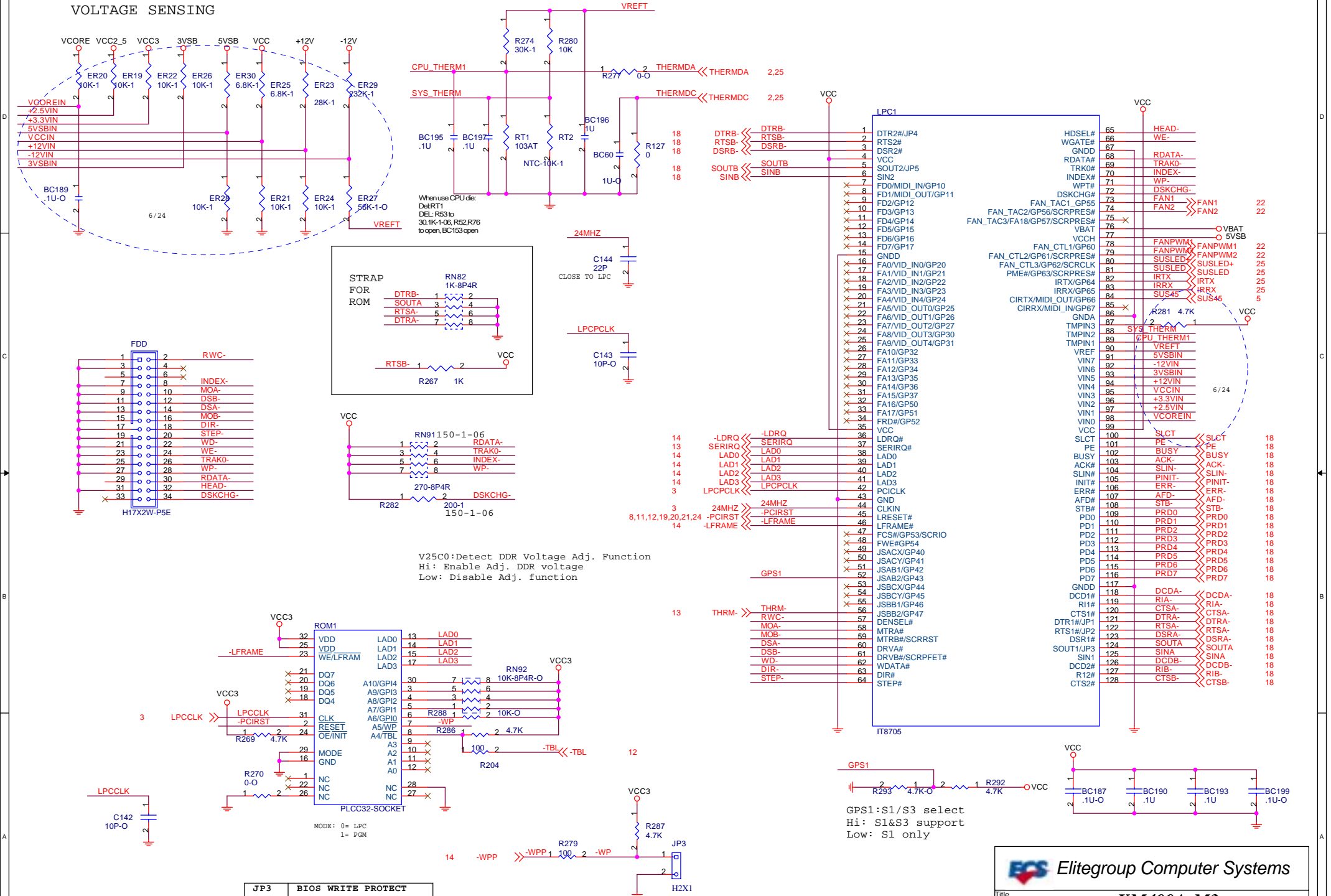
 Elitegroup Computer SystemsTitle *KM400A-M3*

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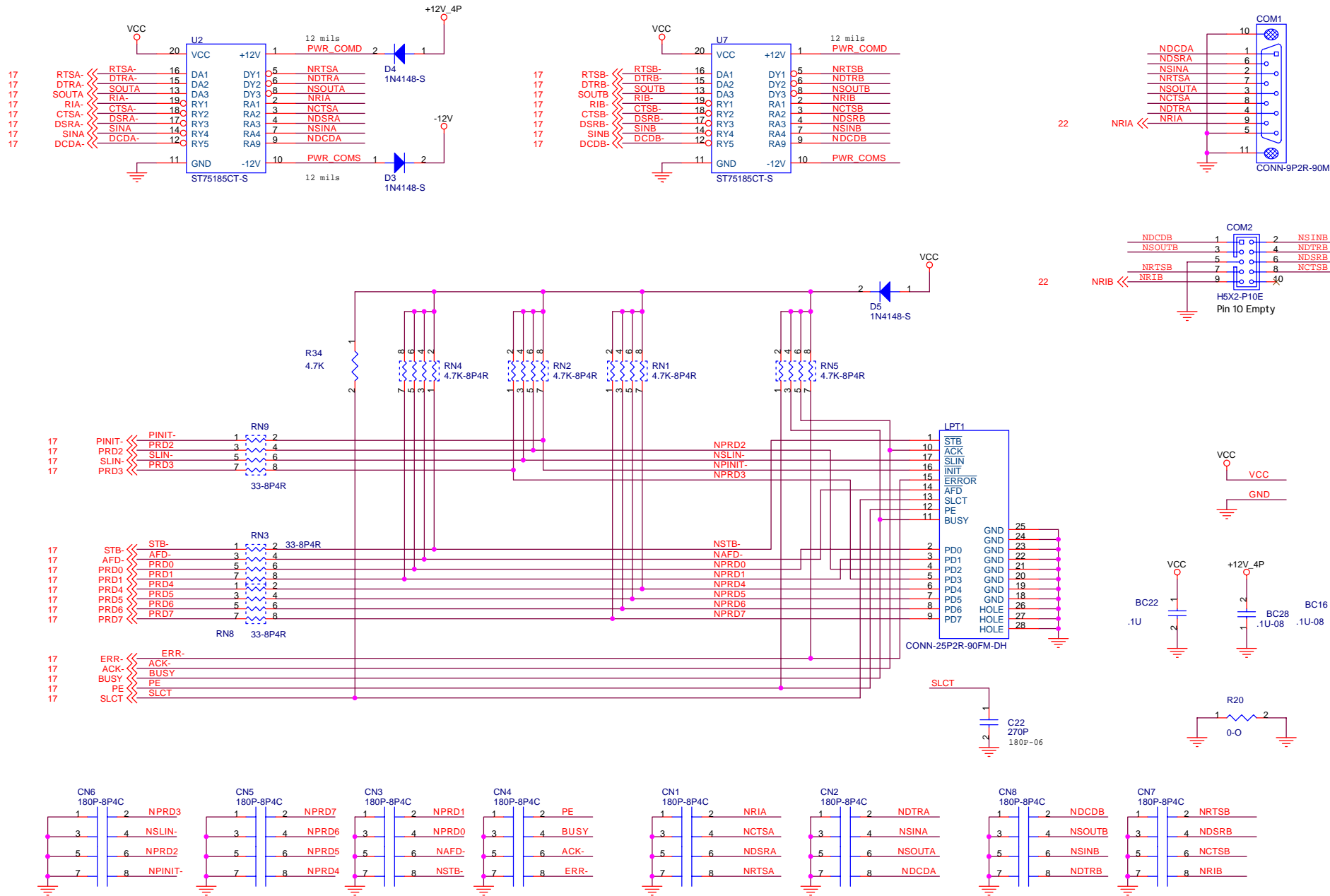
Custom	USB/PS2	A
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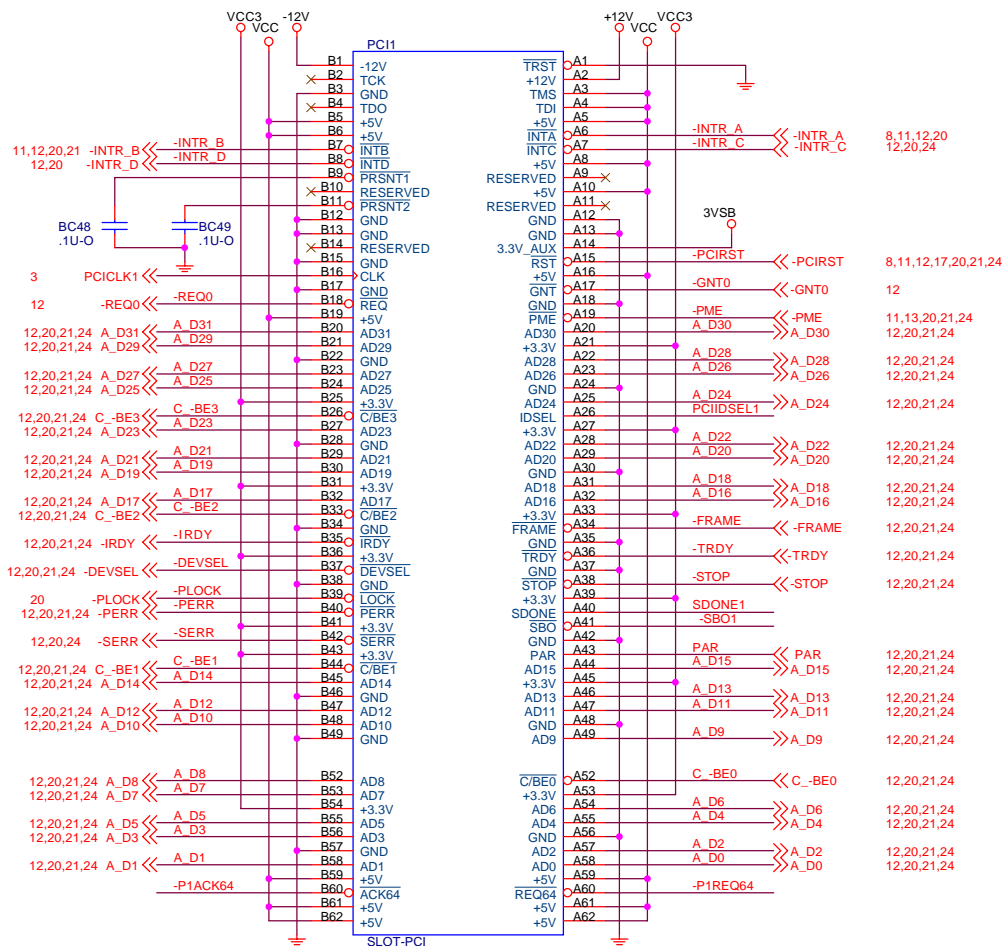
Date:	Thursday, July 01, 2004	Sheet	16	of	27
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## VOLTAGE SENSING



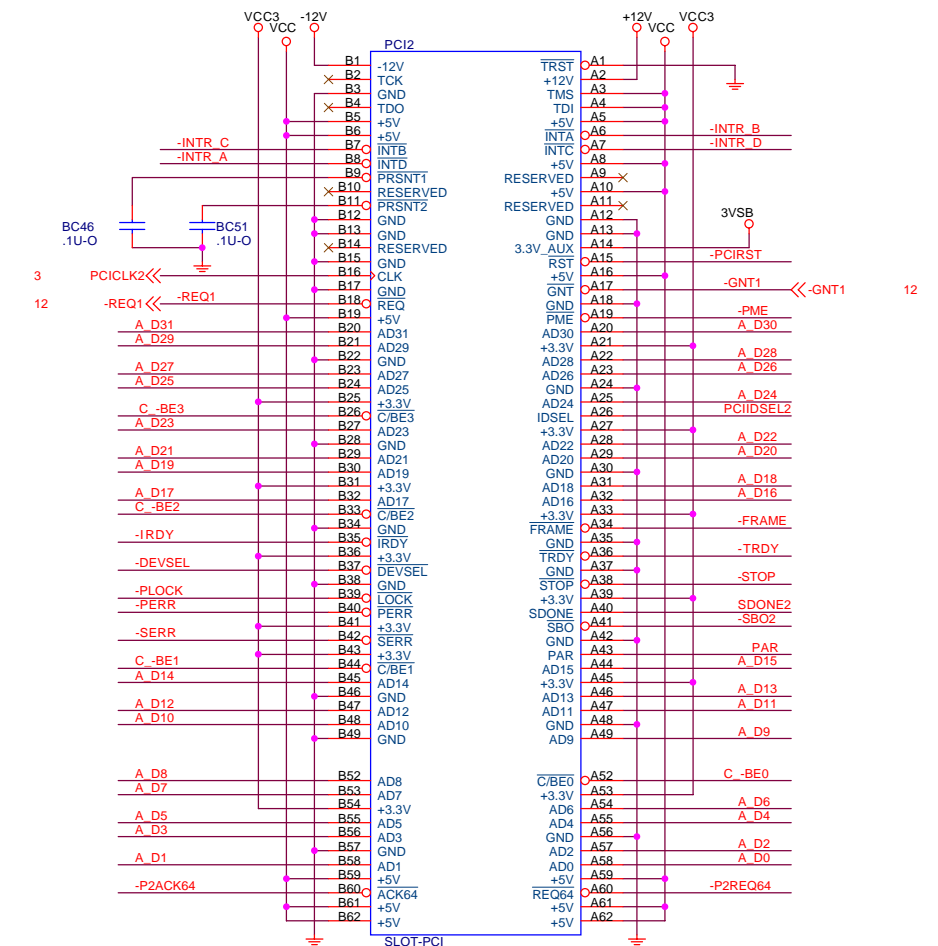
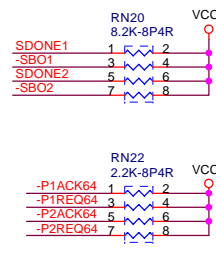
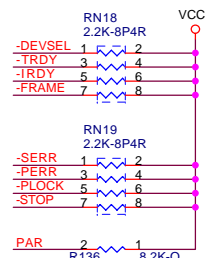
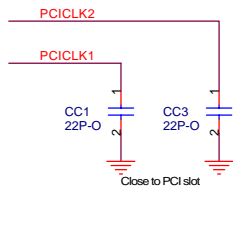
JP3	BIOS WRITE PROTECT
OPEN	WRITE PROTECT DISABLE
SHORT	WRITE PROTECT ENABLE





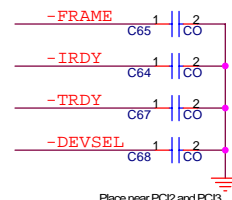
IDSEL=AD19

PCIIDSEL1 2 1 A\_D19 A\_D19 12,20,21,24

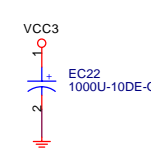
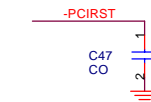


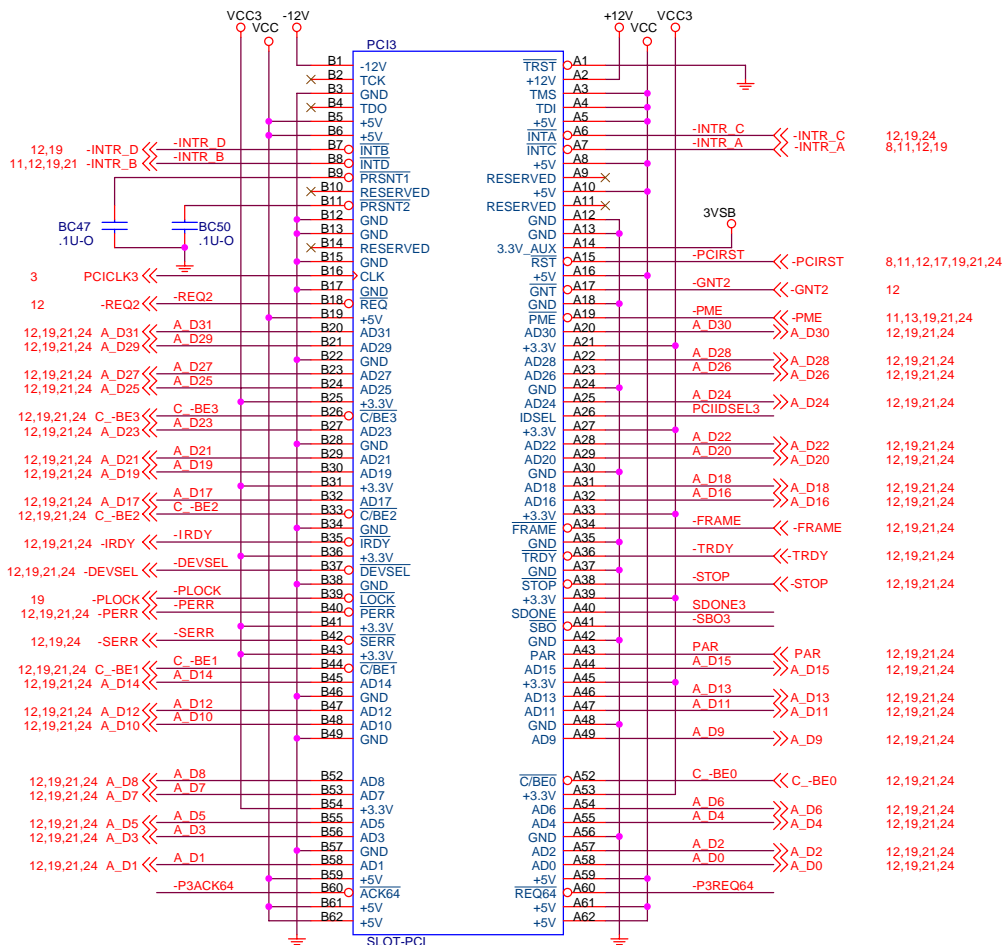
IDSEL=AD20

PCIIDSEL2 2 1 A\_D20 A\_D20 12,20,21,24



Place near PC2 and PC3





### FID Codes

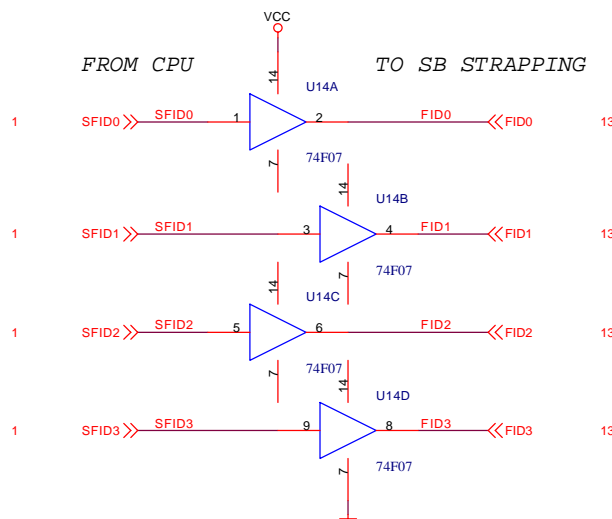
Four-Bit FID	Clock Multiplier	Four-Bit FID	Clock Multiplier
0000	11.0	1000	7.0
0001	11.5	1001	7.5
0010	12.0	1010	8.0
0011	12.5	1011	8.5
0100	5.0	1100	9.0
0101	5.5	1101	9.5
0110	6.0	1110	10.0
0111	6.5	1111	10.5

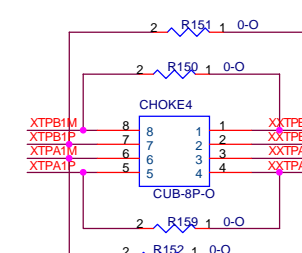
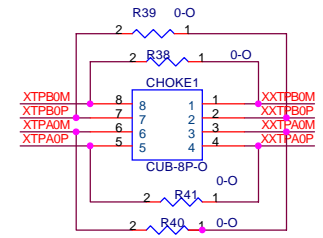
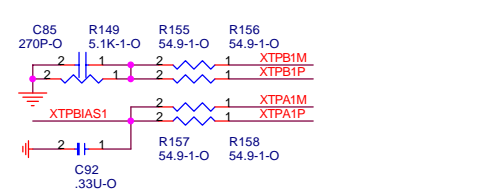
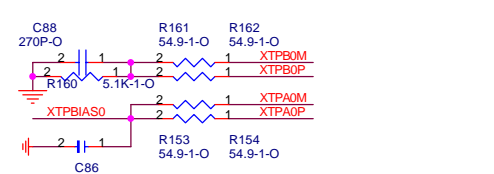
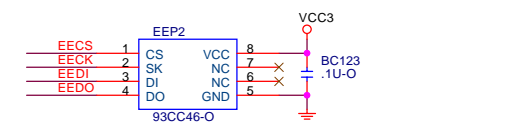
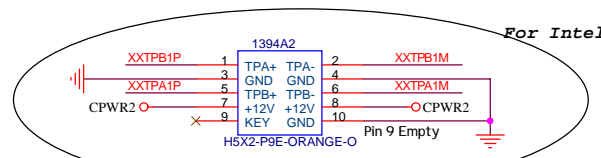
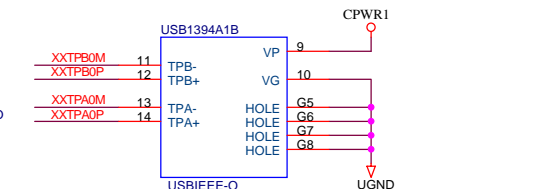
### VID Codes

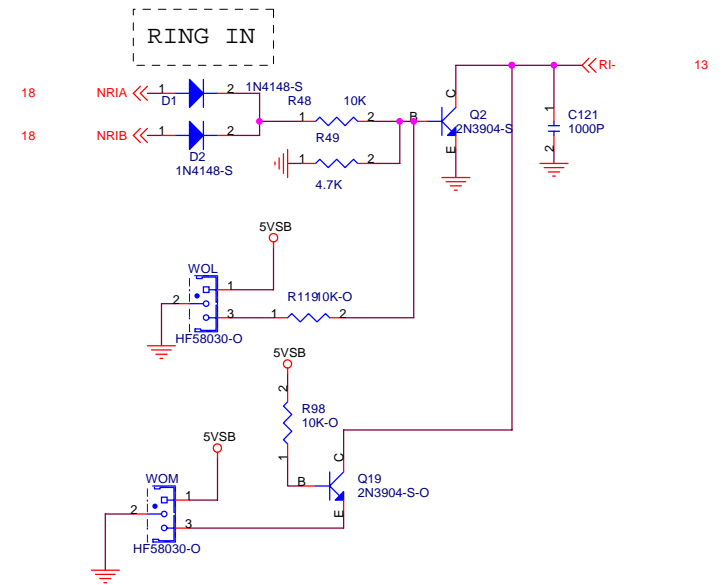
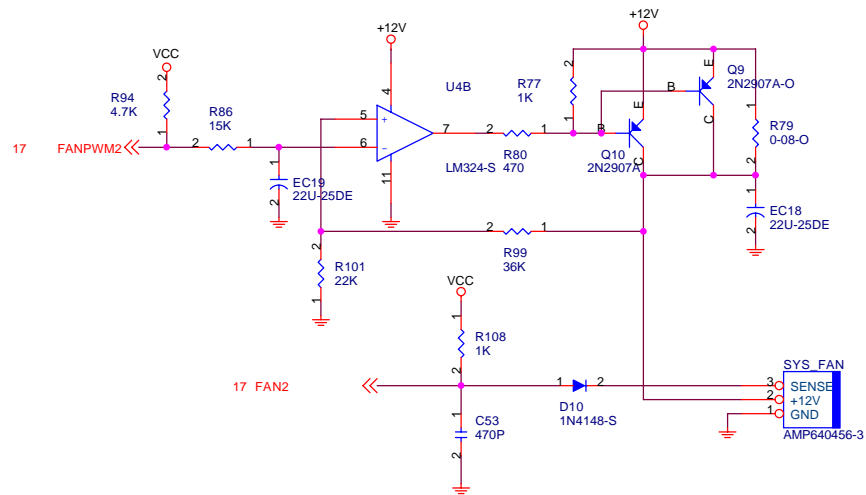
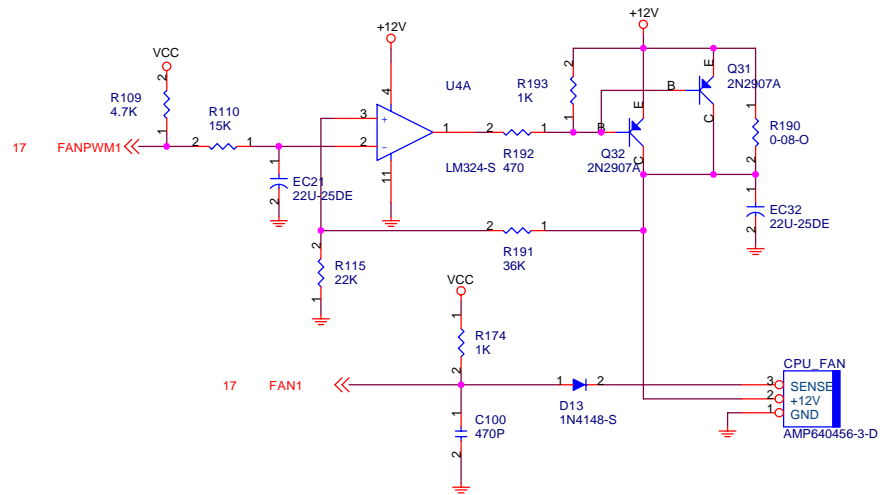
VID[4:0]	VCC_CORE	VID[4:0]	VCC_CORE
00000	1.850	10000	1.450
00001	1.825	10001	1.425
00010	1.800	10010	1.400
00011	1.775	10011	1.375
00100	1.750	10100	1.350
00101	1.725	10101	1.325
00110	1.700	10110	1.300
00111	1.675	10111	1.275
01000	1.650	11000	1.250
01001	1.625	11001	1.225
01010	1.600	11010	1.200
01011	1.575	11011	1.175
01100	1.550	11100	1.150
01101	1.525	11101	1.125
01110	1.500	11110	1.100
01111	1.475	11111	No CPU

FROM CPU

TO SB STRAPPING



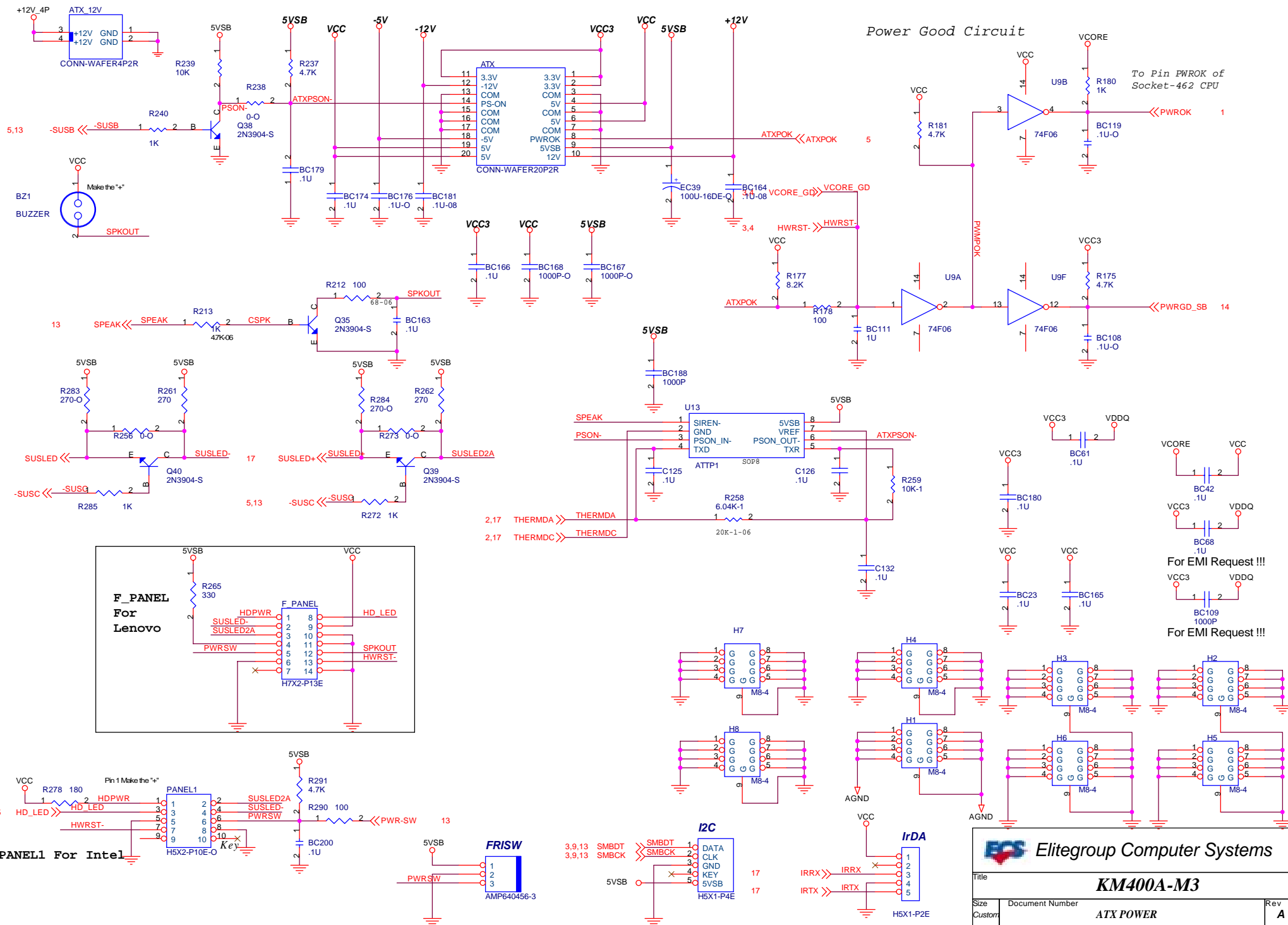






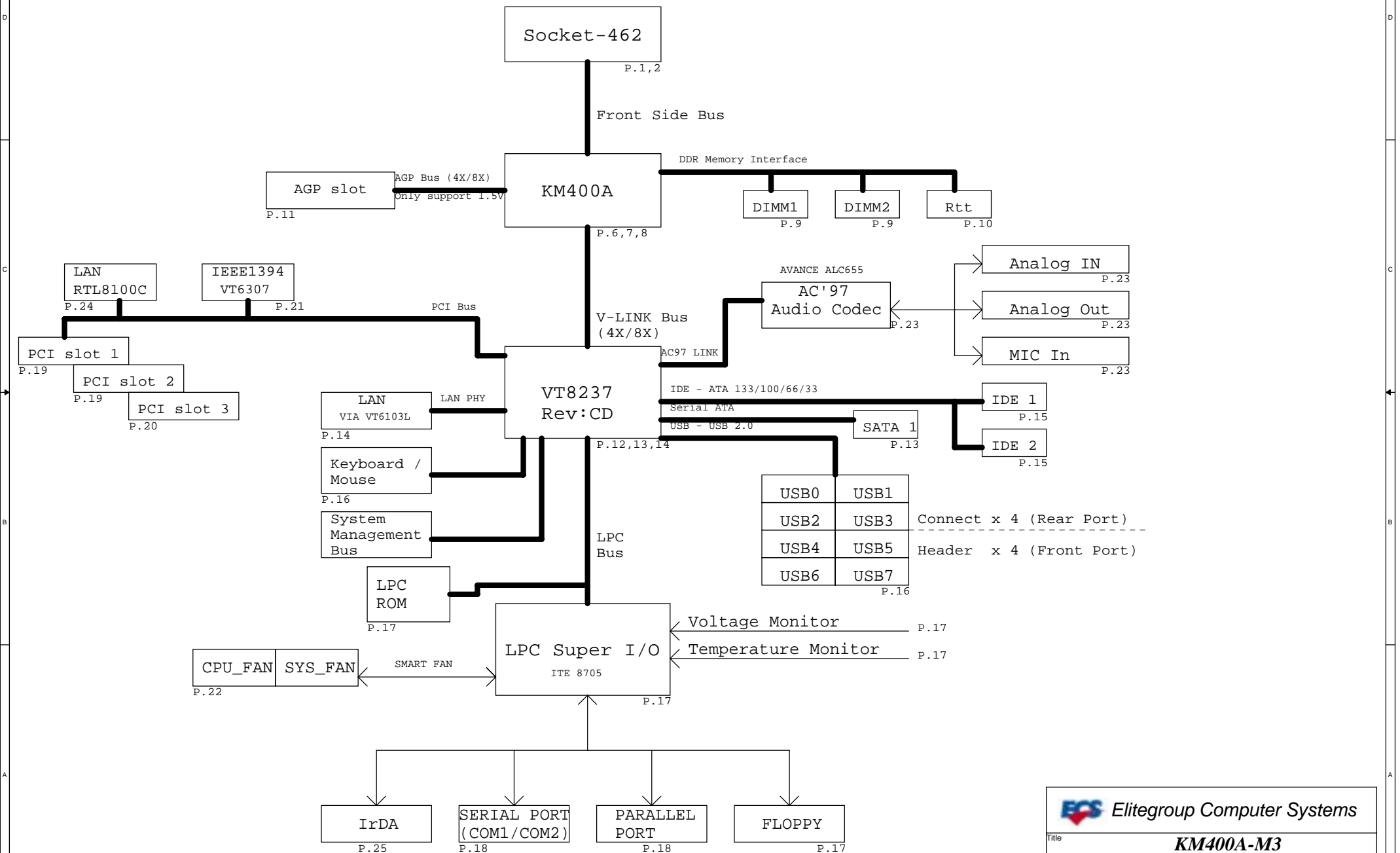






# KM400A-M3

## System Block Diagram






# KM400A-M3

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